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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,610	04/14/2004	Hee-jeon Yang	1572.1247	5084

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EXAMINER

BHAT, ADITYA S

ART UNIT	PAPER NUMBER
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2863

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/823,610

Applicant(s)

YANG ET AL.

Examiner

Aditya S. Bhat

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 4/14/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-14 are rejected under 35 U.S.C. 102(a, e) as being anticipated by Song et al. (USPN 6,487,472).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

With regards to claim 1, Song et al. (USPN 6,487,472) teaches a process control method managing a semiconductor device manufacturing process, including an operation of a system with a plurality of sub-modules, comprising:

diagnosing an operational state of the plurality of sub-modules prior to beginning the semiconductor device manufacturing process; (10;Refer to figure 2)

checking a process condition of the system; (10;Refer to figure 2) and

informing a user of operational states of the sub-modules and the process condition of the system. (Col. 8, lines 17-29)

With regards to claim 2, Song et al. (USPN 6,487,472) teaches a diagnosing an operational state of I/O (input/output) devices of the sub-modules prior to beginning the semiconductor device manufacturing process; and informing the user of the operational state of the input/output devices of the sub-modules. (Col. 7,lines 31-34)

With regards to claim 3, Song et al. (USPN 6,487,472) teaches the diagnosing of the operational state of the plurality of sub-modules includes operating a diagnosis program module to operate a sub-module to perform a diagnosis program. (Col.8, lines 1-4)

With regards to claim 4, Song et al. (USPN 6,487,472) teaches the checking the process condition of the system includes operating a performance diagnosis program module, to check a performance of the system, to perform the performance diagnosis program. (Col.8, lines 1-4)

With regards to claim 5, Song et al. (USPN 6,487,472) checking whether the operational states of the sub-modules and the process condition are normal by comparing a predetermined normal operation value range with a value estimated from a result of the diagnoses of the sub-modules. (Col. 8, lines 32-38)

With regards to claim 6, Song et al. (USPN 6,487,472) teaches selecting, by a user, which object or objects of a plurality of objects are to be diagnosed, prior to beginning the semiconductor device manufacturing process. (Col.7, lines 42-45)

With regards to claim 7, Song et al. (USPN 6,487,472) teaches diagnosing of the sub-modules includes diagnosing a performance condition of equipment based upon at least one of sampled voltage, currents, torques and operational speeds related to the equipment. (Col.8, lines 17-19)

With regards to claim 8, Song et al. (USPN 6,487,472) teaches the equipment comprises system components, including various chambers, a conveyor, and a furnace, and parts of system components, including a valve, a pump, a controller, and a roller, in the semiconductor device manufacturing process. (Refer to figure 7)

With regards to claim 9, Song et al. (USPN 6,487,472) teaches the diagnosing of the operational state of the plurality of sub-modules includes selectively diagnosing some but not all of the plurality of sub-modules. (Col.7, lines 26-29)

With regards to claim 10, Song et al. (USPN 6,487,472) teaches a system for making a semiconductor devices by managing a semiconductor device manufacturing process, including an operation of a system having a plurality of sub-modules, comprising:

a module checking part diagnosing an operational state of at least one sub-module of the plural sub-modules; (10;Refer to figure 2)

a process condition checking part diagnosing a process condition of the system; (10;Refer to figure 2)

a result display displaying a diagnosis result of an object, of a plurality of objects of the system, to be diagnosed; (28a; Refer to figure 9) and

a controller controlling the module, checking part and the process condition checking part to check the operational state of the one sub-module and the process condition of the system prior to beginning the semiconductor device manufacturing process and controlling the display of the result of the diagnosis in the result display. (23a; Refer to figure 9)

With regards to claim 11, Song et al. (USPN 6,487,472) teaches a an interface checking part checking an operational state of an I/O device of the one sub-module, wherein the controller controls the result display to display the result of diagnosis performed by the interface checking part. (28; Refer to figure 4)

With regards to claim 12, Song et al. (USPN 6,487,472) teaches a controller permits a user to select the object or objects, of the plural objects, to be diagnosed. (Col.7, lines 41-45)

With regards to claim 13, Song et al. (USPN 6,487,472) teaches a user is permitted to select objects not to be diagnosed. (Col.7, lines 41-45)

With regards to claim 14, Song et al. (USPN 6,487,472) teaches a computer readable code controlling a system to perform the method of claim 1. (Col.8, lines 1-5)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Naya et al. (USPN 6,591,207), (USPN 6,850,854) teaches a semiconductor production system, Nakamoto et al. (USPUB 2004/0078946), (USPN

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6,901,306) teaches a semiconductor manufacturing apparatus and its diagnosis apparatus and operating system, Nishihata et al. (USPUB 2002/0013908) teaches a remote diagnostic system for facilities and remote diagnostic method, and Shi et al. (USPN 6,839,713) teaches a system and software for database structure in semiconductor manufacturing and method thereof.

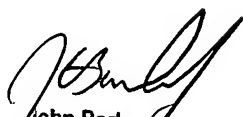
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S. Bhat whose telephone number is 571-272-2270. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aditya Bhat

6/19/05


John Barlow
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